

Web Images Videos Maps News Shopping Gmail more »

Suzanne Lo »



generating probabilistic connection ✕

Search

About 1,310,000 results (0.13 seconds)

[Advanced search](#)

### Everything

[Images](#)

[Videos](#)

[News](#)

[Shopping](#)

[Books](#)

[More](#)

**Alexandria, VA**

[Change location](#)

### All results

[Related searches](#)

[More search tools](#)

#### » Logic Design for On-Chip Test Clock Generation - Implementation ...

by M Beck - 2005 - Cited by 37 - Related articles

Techniques for on-chip clock **generation**, meant to reduce **test** vector count and to ..... Field **programmable** gate arrays (FPGAs) provide **designers** with the ..... that a path's **probabilistic** rank with respect to delay is very different from ..... The first algorithm is a **connection**-based packing technique by which the ...

[portal.acm.org/citation.cfm?id=1049073](http://portal.acm.org/citation.cfm?id=1049073)

#### ATS'97: A test processor chip implementing multiple seed, multiple ...

by ZM Datus - 1997 - Related articles

User **programmable** seed and feedback **connection** can be ... **test** pattern **generation** based on intelligent reseeding of ... **Design** of low cost **test** processor ASIC **chip** employing **probabilistic** approach have already been presented [7, 8, 9]. ...

[doi.ieeecomputersociety.org/10.1109/ATS.1997.643952](http://doi.ieeecomputersociety.org/10.1109/ATS.1997.643952)

#### Syllabus - IEC COLLEGE

Automatic **test** pattern **generation**, **Design** for testability, Scan **design**, .... probability & frequency, **probabilistic** power analysis techniques, signal entropy. .... CMOS **Chip design** Options, **programmable** logic, **Programmable** inter **connect** ...

[ieccollege.com/M-TechSyllabus.asp](http://ieccollege.com/M-TechSyllabus.asp) - Cached

#### Publications

The **Design** of the I-slate is intended to be based on **probabilistic chip design** ... **generation** of a display usually consists of two processes. ... Internet **connection** was also **tested** and used for library installation and simple browsing. ...

[web.iit.ac.in/~jairaj/islite.html](http://web.iit.ac.in/~jairaj/islite.html) - Cached

#### [PDF] Class 217: Introduction to CPLD and FPGA Design, Part 1

File Format: PDF/Adobe Acrobat - Quick View

by S Zeidman - Cited by 5 - Related articles

Introduction to FPGA **Design**. 1. 1. INTRODUCTION. Field **Programmable** Gate Arrays (FPGAs) are ... and **testing** issues that arise when designing an FPGA. ... which transistors to **connect**. First, your low level functions are connected ... simply needs to add the last metal layers to the die to **create** your **chip**, using ...

[pidworld.biz/html/technote/intro.cpld.fpga.design.pdf](http://pidworld.biz/html/technote/intro.cpld.fpga.design.pdf)